This page was produced at ict1301.co.uk for Colin Skelton and there are plans underway to provide this model with a permanent home at TNMOC, whilst this happens here in colin's own words is the history of this unique item.

DM1 by Colin Skelton (16-11-2015) :-

I was de-cluttering my loft when I found a curious small black box, with a model of a computer inside. I then remembered that I had been presented with the model of the DM1 (distributed mainframe) during the heyday of its development.

Rob Wilmott had been appointed Chief Executive of ICL and wanted a small office computer running the VME operating system, with the power of a mainframe but requiring no false floor, fan or air conditioning. It had to be capable of operating as a dual node system, use the fast fibre optic macrolan for disks and slower OSLAN for other peripherals.

A team was formed at ICL West Gorton. Brian Proctor was the architect. Derek Ashcroft led the processor team and Phil Broughton the I/O and store team. Andy Boswell was responsible for the system. Mike Eyre was initially the project manager but shortly after the start he handed that responsibility over to me.

Mainframe computers had previously always been housed in a steel frame, but we had to consider plastic. One very stressful day, the engineer responsible for the physical design, Sid Martin, breezed into my office to boast that he had designed 'the most complex structural foam moulding in Europe' - a challenge I felt we could do without!

To meet the exacting requirements that had been set for us, the recently available LSI technology would be necessary. Brian joined a small group to search the world for a suitable manufacturer. The Japanese Fujitsu 8000 cell CMOS (C8K) process was chosen.

I had been leading the 2966 development and was used to large computers with dozens of printed circuit boards. These often went through many modification levels before functioning properly. It came as a shock to me to learn that we would have to rely on an in-house Design Automation (CAD) system to help us get the design of the chips right first time.

The equivalent of seven 2966 computers were engaged round the clock, seven days a week, for over six months to help us complete the design. This was before the days of broadband, and magnetic tapes would be taken by courier and flown to Japan. Fujitsu would validate the design and deliver to us a prototype chip. Fifteen engineering meetings in Japan were necessary to sort out problems. ICL designed 42 C8K chips, and a typical system would require 60. To my relief, although a few changes were made subsequently, the processing node ran the VME operating system within 5% of expected performance without a single chip design iteration.

DM1 was launched as the ICL Series 39 Level 30 System in 1985.